Distributed by:

JAMECO® ELECTRONICS

**www.Jameco.com ✦ 1-800-831-4242**

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 235230



FAIRCHILD SEMICONDUCTOR™

November 1988
Revised October 2000

# 74AC521 • 74ACT521
# 8-Bit Identity Comparator

## General Description

The AC/ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

## Features

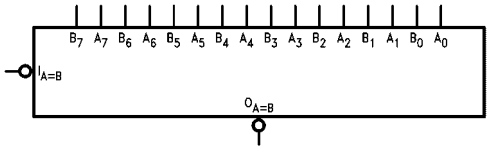
- $I_{CC}$ reduced by 50%
- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- ACT521 has TTL-compatible inputs

## Ordering Code:

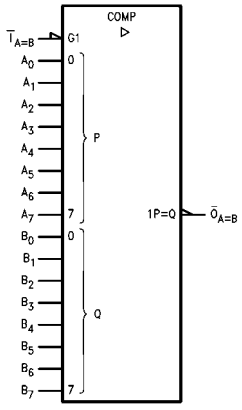
| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC521SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74AC521SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC521MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC521PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| 74ACT521SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACT521SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT521MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT521PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering table.

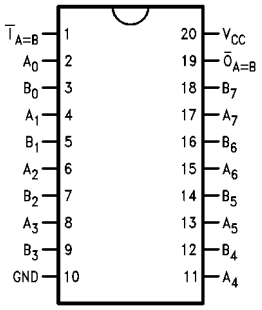
## Logic Symbols




**IEEE/IEC**




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $A_0$–$A_7$ | Word A Inputs |
| $B_0$–$B_7$ | Word B Inputs |
| $T_{A=B}$ | Expansion or Enable Input |
| $\overline{O}_{A=B}$ | Identity Output |

FACT™ is a trademark of Fairchild Semiconductor Corporation.

© 2000 Fairchild Semiconductor Corporation 

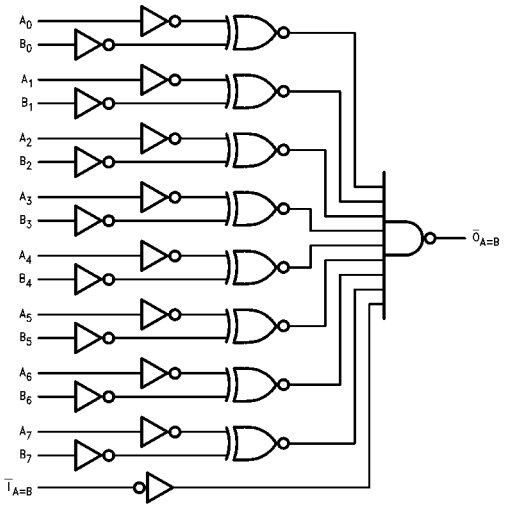
## Truth Table

| Inputs | | Outputs |
|---|---|---|
| $\overline{I}_{A=B}$ | A, B | $\overline{O}_{A=B}$ |
| L | A = B (Note 1) | L |
| L | A ≠ B | H |
| H | A = B (Note 1) | H |
| H | A ≠ B | H |

H = HIGH Voltage Level
L = LOW Voltage Level

**Note 1:** $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

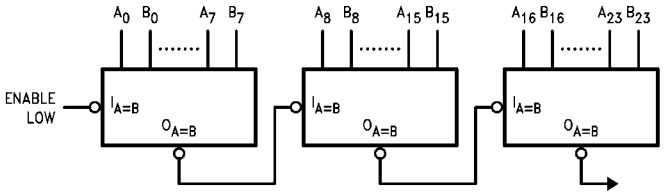
## Logic Diagram



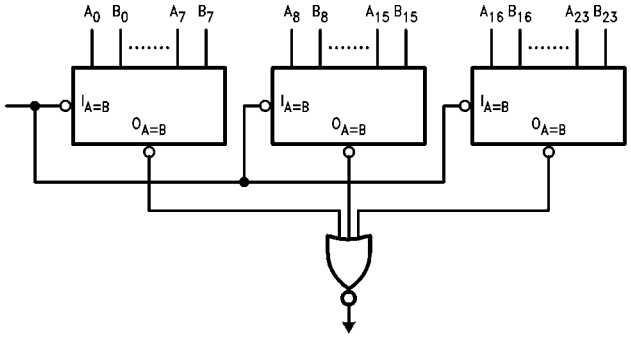

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Applications

**Ripple Expansion**




**Parallel Expansion**



## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source | |
| or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| AC Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C Typ | $T_A$ = −40°C to +85°C Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −50 μA |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 2.56 | 2.46 | | $I_{OH}$ = −12 mA |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 3) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 3) |
| $I_{IN}$ (Note 5) | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 4) | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ (Note 5) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50\ \mu A$ |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OH} = -24$ mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH} = -24$ mA (Note 6) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50\ \mu A$ |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OL} = 24$ mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL} = 24$ mA (Note 6) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 7) | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max |
| $I_{OHD}$ | | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND |

**Note 6:** All outputs loaded; thresholds on input associated with output under test.

**Note 7:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF Min | Typ | Max | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_{A=B}$ | 3.3 | 3.5 | 7.0 | 11.0 | 3.0 | 12.0 | ns |
| | | 5.0 | 2.5 | 5.0 | 8.0 | 2.0 | 9.0 | |
| $t_{PHL}$ | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_{A=B}$ | 3.3 | 4.5 | 7.5 | 11.5 | 3.5 | 12.5 | ns |
| | | 5.0 | 3.0 | 5.5 | 8.5 | 2.5 | 9.0 | |
| $t_{PLH}$ | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 3.3 | 3.0 | 5.5 | 8.0 | 2.5 | 9.0 | ns |
| | | 5.0 | 2.5 | 4.0 | 6.0 | 2.0 | 7.0 | |
| $t_{PHL}$ | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 3.3 | 3.0 | 5.5 | 8.0 | 2.5 | 9.0 | ns |
| | | 5.0 | 2.0 | 4.0 | 6.0 | 2.0 | 7.0 | |

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

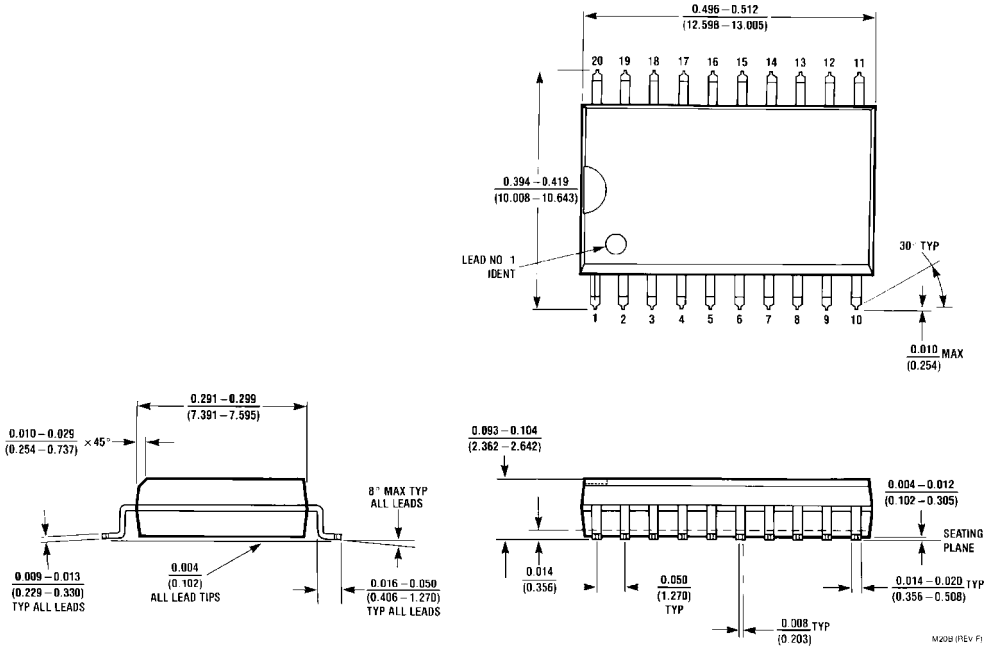
| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_{A=B}$ | 5.0 | 3.0 | 5.5 | 9.0 | 2.5 | 9.5 | ns |
| $t_{PHL}$ | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_{A=B}$ | 5.0 | 3.0 | 6.0 | 10.0 | 2.5 | 11.0 | ns |
| $t_{PLH}$ | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 5.0 | 2.0 | 4.0 | 6.5 | 2.0 | 7.0 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 5.0 | 2.5 | 5.0 | 7.5 | 2.0 | 8.0 | ns |

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

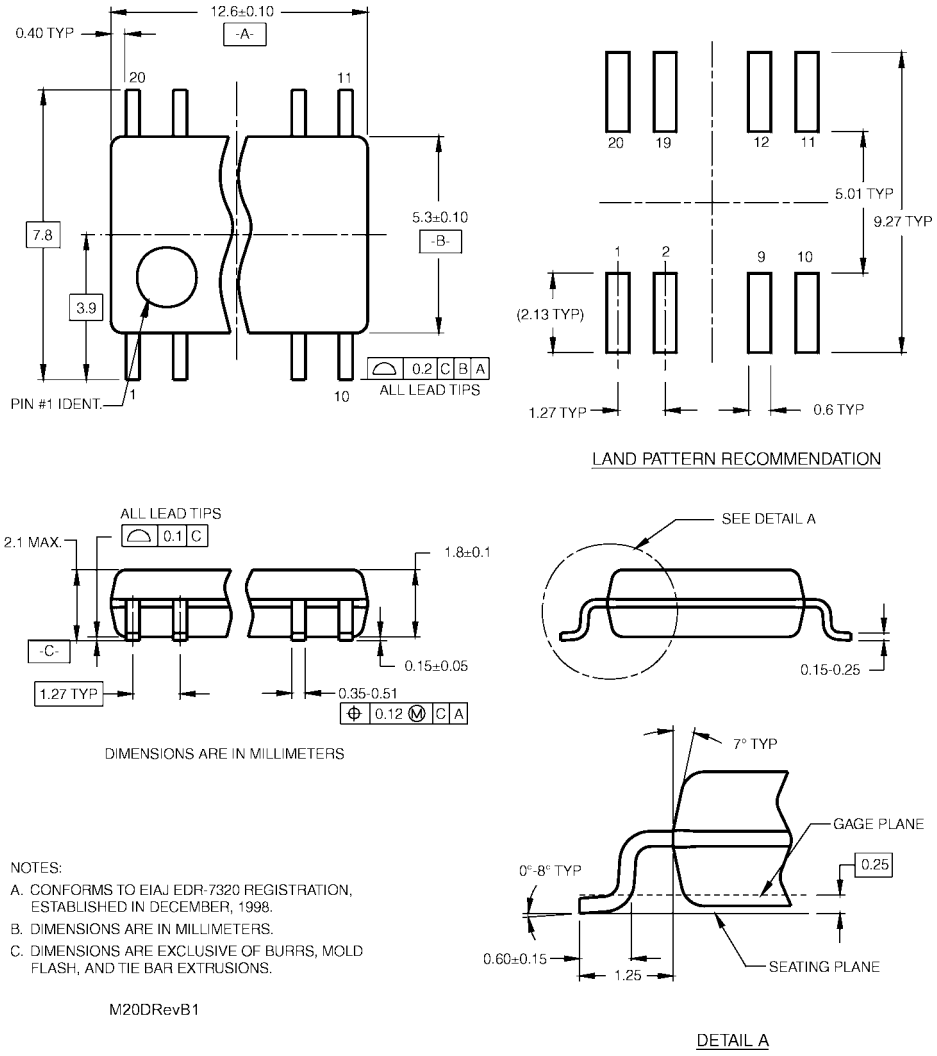
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

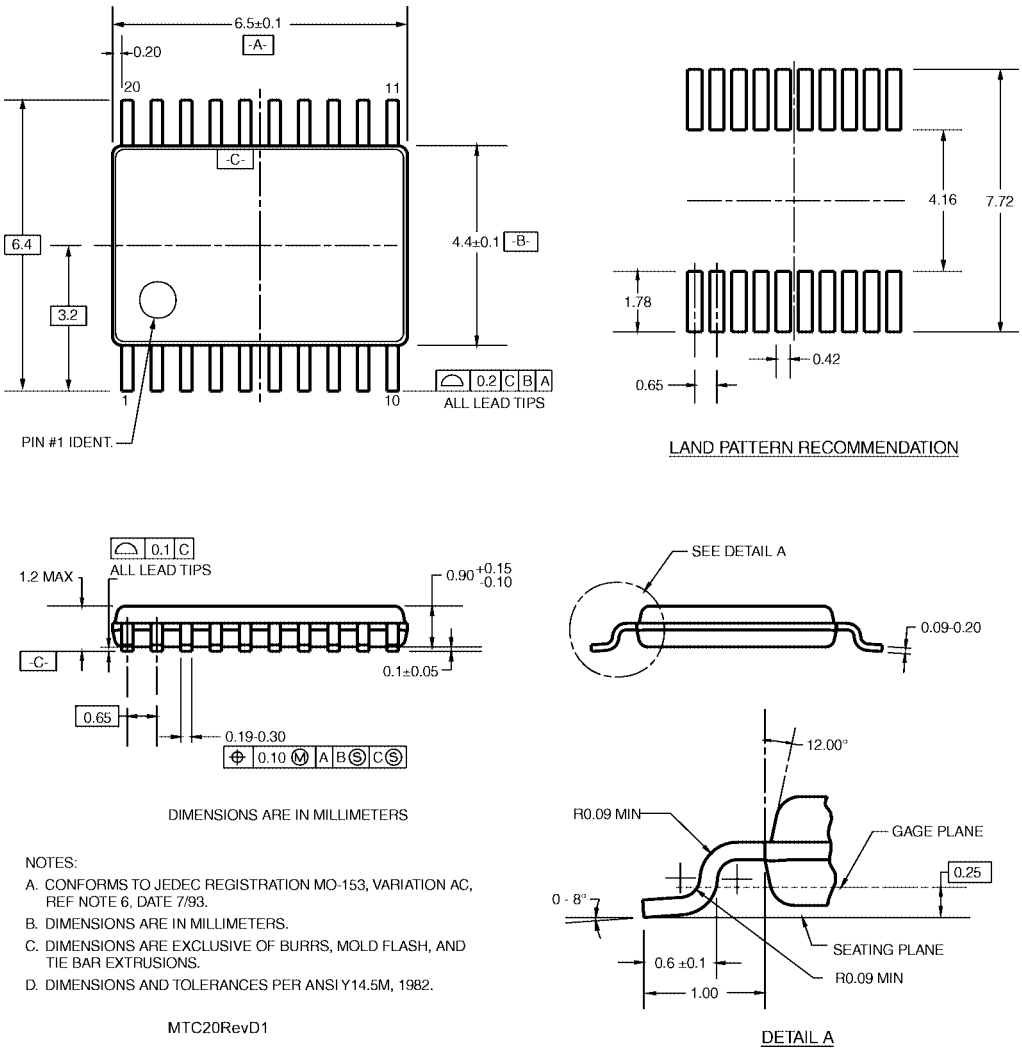
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M20D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

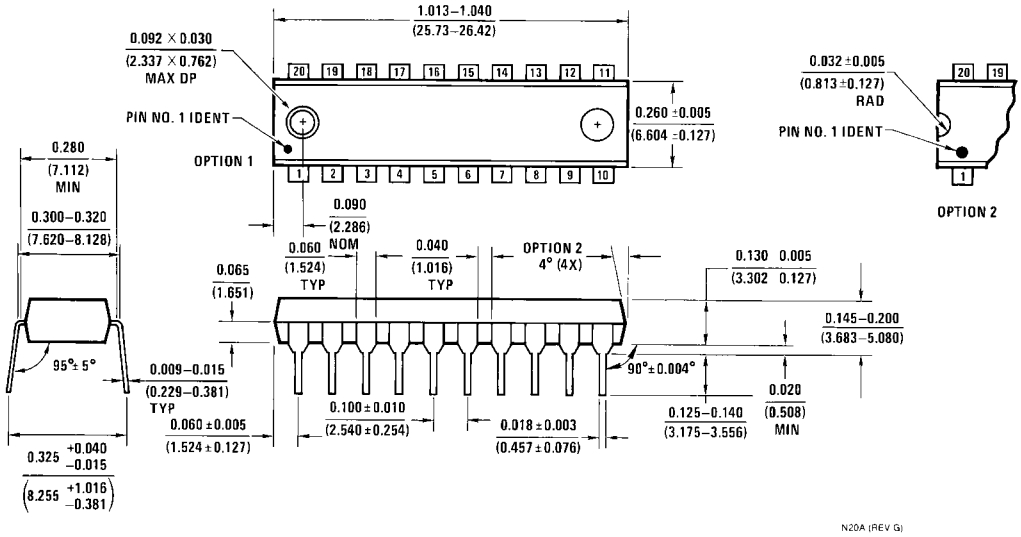
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC20**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**